AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Original) An analog to digital conversion system, comprising:

a plurality of cascaded successive approximation register subconverter stages, the subconverter stages individually comprising:

a switched capacitor system receiving an analog subconverter stage input voltage at a switched capacitor system input node and an intermediate digital signal, the switched capacitor system providing an analog switched capacitor system output signal at a switched capacitor system output node, wherein the switched capacitor system comprises:

a plurality of capacitors, individual capacitors comprising a first terminal coupled to a switched capacitor system intermediate node, and a second terminal; and

a switching system coupled to the second terminals of the plurality of capacitors, the switching system selectively coupling individual capacitors to one of the switched capacitor system input node, the switched capacitor system output node, a first reference voltage, and a second reference voltage;

wherein in a sample mode, the switched capacitor system stores the subconverter stage input voltage in the plurality of capacitors;

wherein in a conversion mode, the switched capacitor system applies the intermediate digital signal to the plurality of capacitors and provides the switched

capacitor system output signal representative of a difference between the subconverter stage input voltage and a value of the intermediate digital signal; and

wherein in a residue amplification mode, the switched capacitor system provides the switched capacitor system output signal representative of a difference between the subconverter stage input voltage and a final value of the intermediate digital signal.

2. (Original) The analog to digital conversion system of claim 1, wherein the subconverter stages individually further comprise:

an amplifier system coupled with the switched capacitor system, the amplifier system amplifying the switched capacitor system output signal and providing an analog subconverter stage residue output signal according to the switched capacitor system output signal;

a comparison system coupled with the amplifier system and providing a comparison signal according to the switched capacitor system output signal; and

a successive approximation system coupled with the switched capacitor system and the comparison system, the successive approximation system providing the intermediate digital signal and a subconverter stage digital output signal according to the comparison signal;

wherein in the conversion mode, the successive approximation system iteratively adjusts the value of the intermediate digital signal according to the comparison signal; and

wherein in the residue amplification mode, the amplifier system amplifies the switched capacitor system output signal by a gain factor using at least one capacitor from the plurality of capacitors to provide an analog subconverter stage residue output signal.

3. (Original) The analog to digital conversion system of claim 2, wherein the switched capacitor systems individually further comprise a mode control system coupled with the switching system, the mode control system providing control signals to the switching system to selectively couple individual capacitors to one of the switched

capacitor system input node, the switched capacitor system output node, the first reference voltage, and the second reference voltage in the sample, conversion, and residue amplification modes.

4. (Original) The analog to digital conversion system of claim 3, wherein at least one of the capacitors is coupled with the switched capacitor system input node in the sampling mode, with one of the first and second reference voltages in the conversion mode, and with the switched capacitor system output node in the residue amplification mode.

5. (Original) The analog to digital conversion system of claim 2, wherein the analog to digital conversion system receives a differential conversion system analog input signal, wherein the individual switched capacitor systems receive a differential analog subconverter stage input voltage at first and second switched capacitor system input nodes and provide a differential analog switched capacitor system output signal at first and second switched capacitor system output nodes, and wherein the switched capacitor systems individually comprise:

a first plurality of capacitors individually comprising a first terminal coupled to a first switched capacitor system intermediate node, and a second terminal coupled to the switching system; and

a second plurality of capacitors individually comprising a first terminal coupled to a second switched capacitor system intermediate node, and a second terminal coupled to the switching system.

6. (Original) The analog to digital conversion system of claim 2, wherein a first subconverter stage receives a conversion system analog input signal as the subconverter stage input voltage, wherein the successive approximation system provides a J-bit subconverter stage digital output signal, J being an integer greater than 1, and wherein the gain factor for the first subconverter stage is less than $2^{(J-1)}$.

7. (Original) The analog to digital conversion system of claim 6, wherein a second subconverter stage receives an analog subconverter stage residue output signal from the first subconverter stage, wherein the successive approximation system of the second subconverter stage provides a K-bit subconverter stage digital output signal, K being an integer greater than 1, and wherein the gain factor for the second subconverter stage is greater than $2^{(K-1)}$.

8. (Original) The analog to digital conversion system of claim 2, wherein the plurality of capacitors have substantially equal capacitance values, and wherein the successive approximation system provides the intermediate digital signal in a thermometer code.

9. (Original) The analog to digital conversion system of claim 1, wherein a first subconverter stage receives a conversion system analog input signal as the subconverter stage input voltage, wherein a first subconverter stage provides a J-bit subconverter stage digital output signal, J being an integer greater than 1, wherein in the residue amplification mode, the first subconverter stage amplifies the switched capacitor system output signal by a gain factor using at least one capacitor from the plurality of capacitors to provide an analog subconverter stage residue output signal, and wherein the gain factor for the first subconverter stage is less than $2^{(J-1)}$.

10. (Original) The analog to digital conversion system of claim 9, wherein a second subconverter stage receives an analog subconverter stage residue output signal from the first subconverter stage, wherein the second subconverter stage provides a K-bit subconverter stage digital output signal, K being an integer greater than 1, wherein the second subconverter stage amplifies the switched capacitor system output signal by a gain factor using at least one capacitor from the plurality of capacitors to provide an analog second subconverter stage residue output signal, and wherein the gain factor for the second subconverter stage is greater than $2^{(K-1)}$.

11. (Original) The analog to digital conversion system of claim 1, wherein the switched capacitor systems individually further comprise a mode control system coupled with the switching system, the mode control system providing control signals to the switching system to selectively couple individual capacitors to one of the switched capacitor system input node, the switched capacitor system output node, the first reference voltage, and the second reference voltage in the sample, conversion, and residue amplification modes.

12. (Original) The analog to digital conversion system of claim 1, further comprising a digital error correction system coupled to the subconverter stages and receiving subconverter stage digital output signals from the subconverter stages, the error correction system providing a conversion system digital output signal according to the subconverter stage digital output signals.

13. (Original) The analog to digital conversion system of claim 1, wherein the analog to digital conversion system receives a differential conversion system analog input signal, wherein the individual switched capacitor systems receive a differential analog subconverter stage input voltage at first and second switched capacitor system input nodes and provide a differential analog switched capacitor system output signal at first and second switched capacitor system output nodes, and wherein the switched capacitor systems individually comprise:

a first plurality of capacitors individually comprising a first terminal coupled to a first switched capacitor system intermediate node, and a second terminal coupled to the switching system; and

a second plurality of capacitors individually comprising a first terminal coupled to a second switched capacitor system intermediate node, and a second terminal coupled to the switching system.

14. (Original) The analog to digital converter of claim 1, wherein the plurality of capacitors have substantially equal capacitance values, and wherein the switching system selectively couples the individual capacitors according to an intermediate digital signal in a thermometer code.

15. (Original) An analog to digital conversion system, comprising:

a first successive approximation subconverter stage comprising a first switched capacitor system including a plurality of capacitors and a switching system that selectively couples individual capacitors to one of a first subconverter stage input node, a first subconverter stage output node, a first reference voltage, and a second reference voltage during sample, conversion, and residue amplification modes, the first subconverter stage receiving an analog input signal, providing a first multi-bit digital output signal representative of the analog input signal, and providing a first subconverter stage residue output signal representative of a difference between the analog input signal and a final value of the first multi-bit digital output signal;

a second successive approximation subconverter stage comprising a second switched capacitor system including a plurality of capacitors and a switching system that selectively couples individual capacitors to one of a second subconverter stage input node, a second subconverter stage output node, the first reference voltage, and the second reference voltage during sample, conversion, and residue amplification modes, the second subconverter stage receiving the first subconverter stage residue output signal, providing a second multi-bit digital output signal representative of the first subconverter stage residue output signal, and providing a second subconverter stage residue output signal representative of a difference between the first subconverter stage residue output signal and a final value of the second multi-bit digital output signal.

16. (Original) The analog to digital conversion system of claim 15, further comprising a digital error correction system coupled to the subconverter stages and receiving the first and second multi-bit digital output signals, the error correction system providing a conversion system digital output signal according to the subconverter stage digital output signals.

17. (Original) The analog to digital conversion system of claim 15, wherein the analog input signal and the first and second residue output signals are differential.

18. (Original) The analog to digital conversion system of claim 15, wherein the first multi-bit digital output signal comprises J bits, J being an integer greater than 1, wherein the first subconverter stage provides the first subconverter stage residue output signal representative of the difference between the analog input signal and the final value of the first multi-bit digital output signal amplified by a first gain factor, and wherein the first gain factor is less than $2^{(J-1)}$.

19. (Original) The analog to digital conversion system of claim 18, wherein the second multi-bit digital output signal comprises K bits, K being an integer greater than 1, wherein the second subconverter stage provides the second subconverter stage residue output signal representative of the difference between the first subconverter stage residue output signal and the final value of the second multi-bit digital output signal amplified by a second gain factor, and wherein the second gain factor is greater than $2^{(K-1)}$.

20. (Original) The analog to digital conversion system of claim 15, wherein the plurality of capacitors of the subconverter stages have substantially equal capacitance values, and wherein the switching systems selectively couple the individual capacitors according to an intermediate digital signal in a thermometer code.

21. (Original) An analog to digital conversion system, comprising:

a plurality of successive approximation subconverter stages, each subconverter stage receiving a subconverter stage analog input signal and providing a subconverter stage digital output signal representative of the subconverter stage analog input signal;

wherein the plurality of successive approximation subconverter stages comprises a first subconverter stage receiving a conversion system analog input signal and providing an analog first residue output signal and a first digital output signal comprising J bits, J being an integer greater than 1, the first residue output signal being representative of a difference between the conversion system analog input signal and a final value of the first digital output signal amplified by a first gain factor, wherein the first gain factor is less than $2^{(J-1)}$.

22. (Original) The analog to digital conversion system of claim 21, wherein the plurality of successive approximation subconverter stages further comprises:

a second successive approximation subconverter stage receiving the first residue output signal and providing an analog second residue output signal and a second digital output signal comprising K bits, K being an integer greater than 1, the second residue output signal being representative of a difference between the first residue output signal and a final value of the second digital output signal amplified by a second gain factor, wherein the second gain factor is greater than $2^{(K-1)}$.

23. (Original) The analog to digital conversion system of claim 22, wherein J=K.

24. (Original) The analog to digital conversion system of claim 21, wherein the plurality of successive approximation subconverter stages individually comprise:

a switched capacitor system receiving an analog subconverter stage input voltage at a switched capacitor system input node and an intermediate digital signal, the switched

capacitor system providing an analog switched capacitor system output signal at a switched capacitor system output node, wherein the switched capacitor system comprises:

a plurality of capacitors, individual capacitors comprising a first terminal coupled to a switched capacitor system intermediate node, and a second terminal; and

a switching system coupled to the second terminals of the plurality of capacitors, the switching system selectively coupling individual capacitors to one of the switched capacitor system input node, the switched capacitor system output node, a first reference voltage, and a second reference voltage;

wherein in a sample mode, the switched capacitor system stores the subconverter stage input voltage in the plurality of capacitors;

wherein in a conversion mode, the switched capacitor system applies the intermediate digital signal to the plurality of capacitors and provides the switched capacitor system output signal representative of a difference between the subconverter stage input voltage and a value of the intermediate digital signal; and

wherein in a residue amplification mode, the switched capacitor system provides the switched capacitor system output signal representative of a difference between the subconverter stage input voltage and a final value of the intermediate digital signal.

25. (Original) The analog to digital conversion system of claim 24, wherein the subconverter stages individually further comprise:

an amplifier system coupled with the switched capacitor system, the amplifier system amplifying the switched capacitor system output signal and providing an analog subconverter stage residue output signal according to the switched capacitor system output signal;

a comparison system coupled with the amplifier system and providing a comparison signal according to the switched capacitor system output signal; and

a successive approximation system coupled with the switched capacitor system and the comparison system, the successive approximation system providing the intermediate digital signal and a subconverter stage digital output signal according to the comparison signal;

wherein in the conversion mode, the successive approximation system iteratively adjusts the value of the intermediate digital signal according to the comparison signal; and

wherein in the residue amplification mode, the amplifier system amplifies the switched capacitor system output signal by a gain factor using at least one capacitor from the plurality of capacitors to provide an analog subconverter stage residue output signal.

26. (Original) The analog to digital conversion system of claim 24, wherein the analog to digital conversion system receives a differential conversion system analog input signal, wherein the individual switched capacitor systems receive a differential analog subconverter stage input voltage at first and second switched capacitor system input nodes and provide a differential analog switched capacitor system output signal at first and second switched capacitor system output nodes, and wherein the switched capacitor systems individually comprise:

a first plurality of capacitors individually comprising a first terminal coupled to a first switched capacitor system intermediate node, and a second terminal coupled to the switching system; and

a second plurality of capacitors individually comprising a first terminal coupled to a second switched capacitor system intermediate node, and a second terminal coupled to the switching system.

27. (Original) The analog to digital conversion system of claim 21, wherein the plurality of capacitors of the switched capacitor systems have substantially equal capacitance values, and wherein the successive approximation system provides the intermediate digital signal in a thermometer code.

28. (Original) The analog to digital conversion system of claim 21, further comprising a digital error correction system coupled to the subconverter stages and receiving subconverter stage digital output signals from the subconverter stages, the error correction system providing a conversion system digital output signal according to the subconverter stage digital output signals.

29. (Original) The analog to digital conversion system of claim 21, wherein J = 3 and the first gain factor is 2.

30. (Currently amended) A pipelined analog to digital conversion system, comprising:

a first successive approximation subconverter stage comprising a first switched capacitor system including a first capacitor array, the first successive subconverter stage receiving a conversion system analog input and providing a first subconverter stage digital output representative of the conversion system analog input and a first residue output representative of a difference between the conversion system analog input and the first subconverter stage digital output; and

a second successive approximation subconverter stage comprising a second switched capacitor system including a second capacitor array, the second~~first~~ successive subconverter stage receiving the first residue output and providing a second subconverter stage digital output representative of the first residue output and a second residue output representative of a difference between the received first residue output and the second subconverter stage digital output.

31. (Original) The pipelined analog to digital conversion system of claim 30, wherein the first and second subconverter stage digital outputs are both multi-bit.